Code No: R201221 **R20** SET - 1

I B. Tech II Semester Regular Examinations, September- 2021

DIGITAL LOGIC DESIGN

(CSE-CS&T, CSE-AI&ML, CSE-AI, CSE-DS, CSE-AI&DS, CSE-CS, CSE-IOT&CS INCL BCT, CSE-CS&BS,CSE-IOT, AI&DS, Cyber Security)

Time: 3 hours Max. Marks: 70

Answer any five Questions one Question from Each Unit
All Questions Carry Equal Marks

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UNIT-I

1 a) Express the following numbers in decimal: (7M)
   (i) $(10110.0101)_2$
   (ii) $(16.5)_{16}$

   b) Perform the subtraction on the given unsigned binary numbers using the 2's complement: (7M)
   (i) 1001-110101
   (ii) 101000-10101

Or

2 a) Perform the subtraction on the given unsigned binary numbers using the 1's complement: (8M)
   (i) 10011-10010
   (ii) 100010-100110

   b) Represent the decimal number 6,428 in: (i) BCD, (ii) excess-3 code, (iii) 2421 code. (6M)

UNIT-II

3 a) Express the following function in sum of min terms and product of max terms: (7M)
F(x, y, z) = (xy+z) (xz+y).

   b) Simplify the Boolean function together with the don't care conditions using K-map method: (7M)
F(A,B,C,D)=Σ(3,4,13,15); d(A,B,C,D)=Σ(1,2,5,6,8,10,12,14).

Or

4 a) Simplify the following expression and implement with two-level NAND gate circuits: (7M)

AB′+ABD+ABD′+A′C′D′+A′BC′

   b) Simplify the Boolean function using K-map in products of sums form: (7M)
F(w,x,y,z)=Σ(2,3,10,11,12,13,14,15).

UNIT-III

5 a) Draw the logic diagram of a 2-to-4-line decoder with only NOR gates. (7M)

   b) Write a HDL model of the 4-bit binary to gray code converter. (7M)

Or

6 a) Write a hierarchical gate-level HDL model of the 16x1 multiplexer. (7M)

   b) Implement the following Boolean functions with a PROM: (7M)
A(x,y,z)=Σ(1,2,4,6); B(x,y,z)=Σ(0,1,6,7); C(x,y,z)=Σ(2,6); D(x,y,z)=Σ(1,2,3,5,7).
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UNIT-IV

7	a)	Explain the principle of RS Flip-flop with the help of logic diagram and truth table.	(7M)
	b)	Convert the T Flip-flop into JK Flip-flop.	(7M)

Or

8	a)	Explain the principle of D Flip-flop with the help of logic diagram and excitation table.	(7M)
	b)	Convert the JK Flip-flop into RS Flip-flop.	(7M)

UNIT-V

9	a)	Explain the operation of 4-bit universal shift register with D flip-flops.	(7M)
	b)	Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6. Use JK flip-flops. Treat the un-used states as don't-care conditions.	(7M)

Or

10	a)	Design a Johnson counter for ten timing signals.	(7M)
	b)	The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift?	(7M)